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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,568	01/13/2004	Seiki Ogura	HALO99-006BB	3526

7590 09/26/2005

George O. Saile
28 Davis Avenue
Poughkeepsie, NY 12603

EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/756,568	OGURA ET AL.
	Examiner	Art Unit
	Thong Q. Le	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *81-83 and 87-95* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *81-83* is/are rejected.

7)☒ Claim(s) *87-95* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on August 25, 2005 has been entered.

2. Claims 1-80, 84-86 have been canceled.

3. Claims 87-95 have been added.

4. Claims 81-83, 87-95 are presented for examination.

Response to Arguments

5. Applicant's arguments, filed 08/25/2005, with respect to the rejection(s) of claim(s) 1-86 under double patenting rejection have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Ogura et al. Pub. No. 2002/0045319.

Double Patenting

6. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

7. Claims 81-83 provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 81-83 of copending Application No. 09/839,966. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Regarding claim 81, Orgura et al. (09/839,966) discloses a method of reading a MONOS memory cell, wherein the MONOS memory cell comprises: a word gate on the surface of a semiconductor substrate; sidewall control gates on sidewalls of said word gate, separated from said word gates by an insulating layer; nitride regions within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions; a polysilicon word line overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and bit line diffusions within said semiconductor substrate adjacent to each of said sidewall control gates wherein one of said nitride regions is a selected nitride region, and the other of said nitride regions is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion, wherein a read operation of said cell is performed by: over-riding said unselected nitride region; providing a voltage on said word gate having a sum of the word gate threshold voltage, an overdrive voltage, and the voltage on said source diffusion; providing a voltage on said control gate adjacent to said selected nitride region sufficient to allow for reading of the selected nitride region; and reading said cell by measuring the voltage level on said bit diffusion (Claim 81).

Regarding claim 82, Orgura et al. (09/839,966) disclose a method of programming a MONOS memory cell, wherein said MONOS memory cell comprises: a word gate on the surface of a semiconductor substrate; sidewall control gates on

sidewalls of said word gate, separated from said word gates by an insulating layer; nitride regions within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions; a polysilicon word line overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and bit line diffusions within said semiconductor substrate adjacent to each of said sidewall control gates; wherein one of said control gates is a selected control gate and its underlying nitride region is a selected nitride region, and the other of said control gates is an unselected control gate and its underlying nitride region is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion, wherein said method of programming the cell comprises the steps of: providing a high voltage on said unselected control gate to over-ride said unselected nitride region', and varying a voltage on said selected control gate (Claim 82)

Regarding claim 83, Orgura et al. (09/839,966) disclose a method of erasing a MONOS memory cell, wherein said MONOS memory cell comprises: a word gate on the surface of a semiconductor substrate; sidewall control gates on sidewalls of said word gate, separated from said word gates by an insulating layer; nitride regions within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions; a polysilicon word line overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and bit

line diffusions within said semiconductor substrate adjacent to each of said sidewall control gates; wherein said method of erasing a block of said nitride regions comprises the steps of: providing a first voltage to said bit line diffusions; and providing a second voltage opposite to said first voltage to said control gate over said bit line diffusions (Claim 83).

Allowable Subject Matter

8. Claims 87-95 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 87-95 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Orgura et al. (09/839,966) and others, does not teach the claimed invention having applying a control gate voltage of 0 volts to all cells beside the cell desired to be read.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827